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140	7590 06/21/2006		EXAMINER	
LADAS & PARRY 26 WEST 61ST STREET			JEFFERSON, QUOVAUNDA	
NEW YORK, NY 10023			ART UNIT	PAPER NUMBER .
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Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)	10
		10/542,123	POPOV ET AL.	
	Office Action Summary	Examiner	Art Unit	
		Quovaunda Jefferson	2823	
Period fo	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the	correspondence addr	'ess
A SH WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DATE of time may be available under the provisions of 37 CFR 1.1. SIX (6) MONTHS from the mailing date of this communication. In period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATIO 36(a). In no event, however, may a reply be ti will apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	N. mely filed the mailing date of this come (ED (35 U.S.C. § 133).	
Status				
2a)□	Responsive to communication(s) filed on <u>09 De</u> This action is <b>FINAL</b> . 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final.		nerits is
Dispositi	on of Claims			
5)□ 6)⊠ 7)□ 8)□	Claim(s) <u>1-9</u> is/are pending in the application.  4a) Of the above claim(s) is/are withdray Claim(s) is/are allowed.  Claim(s) <u>1-9</u> is/are rejected.  Claim(s) is/are objected to.  Claim(s) are subject to restriction and/o			
	on Papers			
10)	The specification is objected to by the Examine The drawing(s) filed on is/are: a) accomplicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Example 2.	epted or b) objected to by the drawing(s) be held in abeyance. Se ion is required if the drawing(s) is ob	e 37 CFR 1.85(a). pjected to. See 37 CFR	
Priority u	ınder 35 U.S.C. § 119			
12)⊠ a)[	Acknowledgment is made of a claim for foreign  All b) Some * c) None of:  1. Certified copies of the priority documents  2. Certified copies of the priority documents  3. Copies of the certified copies of the priority documents  application from the International Bureau  See the attached detailed Office action for a list	s have been received. s have been received in Applicat rity documents have been receiv u (PCT Rule 17.2(a)).	tion No ed in this National St	tage
2) Notic	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail	oate	450
	mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date <u>December 2005</u> .	5)  Notice of Informal I	Patent Application (PTO-1	.DZ)

#### **DETAILED ACTION**

### Specification

A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter. An example is shown on page 2 in the last paragraph in the sentence "the second wafer thermal oxide has a thickness of  $0.2 \div 0.5 \ \mu m$ ". Instead, of the symbol "÷", this symbol should be "-". **Note**: this is not inclusive of all the grammatical and idiomatic errors.

#### Claim Objections

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

The term "bound state" in claim 1 is a relative term, which renders the claim indefinite. The term "bound state" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Examiner is unsure

what the claim means in using the term "bound state" when referring to the implanted hydrogen. Examiner is unsure if this is meant to imply that the implanted hydrogen is remaining in the substrate and is not released into the atmosphere during the drying or annealing phase or could this mean another phenomena.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan, US Patent 6,274,459 in view of Okuchi et al, US Patent 6,286,524.

Regarding claim 1, Chan teaches a method for producing a silicon-on-insulator structure including hydrogen implantation in silicon wafer (column 6, lines 57-61 and column 7, lines 7-16 and figure 2), chemical treatment of silicon wafer and substrate (column 7, lines 54-59. Note: while Chan teaches this cleaning process is done by one wafer, it is well known in the art that the cleaning process can be performed on both the transferring and receiving substrates in order to remove contaminates), joining of silicon

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wafer 2100 and substrate 2201 (figure 4), and splicing and splitting of wafer along the implanted layer (column 8, lines 24-32 and figures 4 and 5), characterized in that a drying, removing of the of physically adsorbed substances from the surfaces of the wafers after chemical treatment is carried out at the moderate temperatures at which the implanted hydrogen is staying in the in the bound state (column 7, lines 59-60. Note: Chan teaches that in hydrogen implantation into silicon has a critical diffusion temperature of 500°C, in which a temperature above this would cause the hydrogen to escape into the atmosphere. Therefore, in order to keep the hydrogen in the substrate, all processes performed before the separation phase would have to be lower than 500°C), and joining the wafer and substrate, their splicing and exfoliating hydrogen induced transferring along the implanted layer in the wafer (column 8, lines 24-32 and figures 4 and 5).

Chan fails to teach a drying is carried out in the low vacuum conditions and splicing and exfoliating hydrogen induced transferring along the implanted layer in the wafer in the same low vacuum conditions at the same or slightly higher moderate temperatures at which the implanted hydrogen is staying mostly in the bound state.

Okuchi teaches a drying is carried out in the low vacuum conditions as part of a process that makes it possible to speed up the intended wafer drying process (column 12, lines 3-9).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Okuchi with that of Chan because the low vacuum condition is part of a process that makes it possible to speed up the intended wafer drying process (column 12, lines 3-9).

Chan and Okuchi fail to teach splicing and exfoliating hydrogen induced transferring along the implanted layer in the wafer in the same low vacuum conditions at the same or slightly higher moderate temperatures at which the implanted hydrogen is staying mostly in the bound state. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 3, Chan further teaches in that the hydrogen implantation is carried out with  $H_2^{\dagger}$  or  $H_2^{\dagger}$  ions with doses (1.5-15) x  $10^{16}$  cm<sup>2</sup> and energies 20 to 200 keV, respectively (column 6, lines 26-31).

Regarding claim 5, Chan further teaches that a touch chemical-mechanical polishing (CMP) or thermal oxidation with following chemical etching in diluted hydrofluoric acid are carried out for removing of upper rough layer on the surface of exfoliated silicon film (column 9, lines 53-67).

Regarding claim 7, Chan further teaches that the substrate is a glass wafer (column 7, line 44), but fails to teach the substrate with the thickness about 500 µm. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re* <u>Woodruff</u>, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 8, Chan further teaches that the substrate is a quartz wafer, but fails to teach the substrate with the thickness about 500 µm. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or

workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 9, Chan fails to teach the drying and splicing and exfoliating along the implanted layer at the temperatures 80 to 350°C with duration from 0.1 to 100 hours are carried out in the low vacuum conditions (10¹ to 10⁴ Pa). However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan in view of Okuchi as applied to claim1 above, and further in view of Eklund et al, US Patent 5,077,228.

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Regarding claim 2, Chan further teaches the method according to claims, characterized in that the hydrogen implantation was carried out through (column 6, line 6), but Chan and Okuchi fails to teach thermally grown oxide SiO<sub>2</sub> with the thickness 5 to 50 nm and following it is removed after implantation. Eklund teaches teach thermally grown oxide SiO<sub>2</sub> with the thickness 5 to 50 nm and following it is removed after implantation (column 3, lines 24-41 and column 4, lines 32-41) because the SiO<sub>2</sub> layer is a sacrificial layer, which is used is formed and removed to remove damage on the surfaces of the trench and provide a high quality surface for the formation of the gate oxide layer.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Eklund with that of Chan and Okuchi because the SiO<sub>2</sub> layer is a sacrificial layer, which is used is formed and removed to remove damage on the surfaces of the trench and provide a high quality surface for the formation of the gate oxide layer (column 4, lines 32-41).

Regarding claim 6, Chan and Okuchi fail to teach that the thickness of thermally grown oxide SiO<sub>2</sub> with on the substrate is equal to 0.01 to 3 µm. Eklund teaches that the

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thickness of thermally grown oxide  $SiO_2$  with on the substrate is equal to 0.01 to 3  $\mu$ (column 3, lines 24-41 and column 4, lines 32-41) because the  $SiO_2$  layer is a sacrificial layer, which is used is formed and removed to remove damage on the surfaces of the trench and provide a high quality surface for the formation of the gate oxide layer.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Eklund with that of Chan and Okuchi because the SiO<sub>2</sub> layer is a sacrificial layer, which is used is formed and removed to remove damage on the surfaces of the trench and provide a high quality surface for the formation of the gate oxide layer (column 4, lines 32-41).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan in view of Okuchi as applied to claim 1 above, and further in view of Aga et al, US Patent 6,846,718. Chan fails to teach a thermal annealing is carried out at 1100° C during 0.5 to 1 hour after splitting. Aga teaches a thermal annealing is carried out after splitting as a means to flatten the delaminated surface (column 2, lines 1-7).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Aga with that of Chan because the thermal annealing is

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carried out after splitting as a means to flatten the delaminated surface (column 2, lines 1-7).

Chan and Aga fails to teach a thermal annealing is carried out at 1100° C during 0.5 to 1 hour after splitting. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo Patent Examiner Art Unit 2823

qvj